REMARKS

Claims 6-9 and 11-15 are pending in the present application. Claims 4, 5 and 10 have been canceled. Replacement claims 6, 7 and 9 have been presented herewith. Also, claims 11-15 have been presented herewith.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document in parent application Serial No. 09/038,749.

Drawings

Applicant notes the Examiner's acceptance of the formal drawings filed along with the present application on January 25, 2001.

Claim Rejections-35 U.S.C. 112

Claims 4 and 5 have been rejected under 35 U.S.C. 112, second paragraph. Although Applicant does not necessarily concede that this rejection is proper, claims 4 and 5 have been canceled to expedite prosecution of this application.

Claim Rejections-35 U.S.C. 102

Claims 4 and 5 have been rejected under 35 U.S.C. 102(b) as being clearly anticipated by the Seeds et al. reference (U.S. Patent No. 3,913,211). However, as noted above, claims 4 and 5 have been canceled.

Claims 6-10 have been rejected under 35 U.S.C. 102(b) as being clearly anticipated by the Seeds et al. reference. This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 6 includes in combination first and second gates "formed on active regions of a substrate", a field oxide "formed on the substrate between said first and second gates", and side walls "formed on side surfaces of said first and second gates". The protective layer is formed on the field oxide, and the insulating layer is formed on the substrate including the first and second gates, the side walls, the field oxide and the protective layer. Applicant respectfully submits that the Seeds et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has alleged that the Seeds et al. reference discloses all the features as set forth in the claims. However, first and second gates are not illustrated in any of Figs. 1a-1h and 2 of the Seeds et al. reference. Also, contrary to the Examiner's assertion, the Seeds et al. reference does not include side walls formed on side surfaces of a gate, or more particularly on first and second gates as now featured in claim 6. Also, the Seeds et al. reference does not disclose an insulating layer formed on a substrate including first and second gates. Accordingly, Applicant respectfully

submits that the semiconductor device of claim 6 distinguishes over the Seeds et al. reference as relied upon by the Examiner, and that this rejection of claims 6-9 is improper for at least these reasons.

Claims 11-15

An object of the present application is to provide a semiconductor device having field oxide regions for device isolation, whereby the field oxide regions are protected from over etching by a protective layer formed thereon. As particularly described in the Description of the Related Art section on page 4 of the present application with respect to Fig. 2(e), when oxide layer 36 and field oxide layer 34 are simultaneously etched, field oxide layer 34 is reduced in thickness. Accordingly, a field isolation voltage of field oxide layer 34 decreases, so that inter-device leakage current undesirably increases.

Claim 11 includes in combination the features of claim 6 as pending in the Preliminary Amendment dated January 25, 2001, and the features of dependent claim 8 as pending the Preliminary Amendment. The protective layer of claim 11 is featured as being formed on the field oxide only. Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose or make obvious these features.

As emphasized above, an object of the present application is to provide a protective layer over the field oxide, to prevent over etching and the resultant increase of inter-device leakage current. In contrast, an object of Seeds et al. reference as described in column 2, lines 16-20 therein, is to retain a gate oxide on the device

throughout processing, so that a surface of the device is protected and contaminants and other impurities are prevented from forming on the surface of the semiconductor material.

As described beginning in column 4, line 26 of the Seeds et al. reference with respect to Figs. 1e and 1f, polycrystalline silicon layer 17 is formed after opening 12b is formed in gate oxide 12. Thus, a part of polycrystalline silicon layer 17 contacts the surface of substrate 11. As further described in column 4, lines 50-58 of the Seeds et al. reference, polycrystalline silicon layer 17d is doped and serves as a conductive lead to the active region in substrate 11 beneath opening 12b in gate oxide 12.

Accordingly, contrary to the Examiner's assertion, the Seeds et al. reference does not include a protective layer that is formed on a field oxide only. Clearly, polycrystalline silicon layers 17d and 17a are not protective layers, but are respectively a conductive lead and a gate. For this reasons, polycrystalline silicon layer 17d is not confined to being formed on an oxide layer as featured in claim 11, but is also formed on the substrate as a conductive lead. Accordingly, Applicant respectfully submits that the semiconductor device of claims 11-15 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner, for at least the above reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the

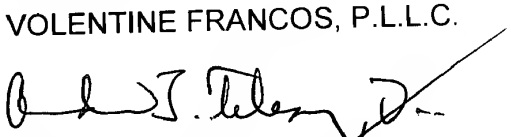
corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



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Enclosures: Version with marked-up changes

VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Claims:

6. (Amended) A semiconductor device comprising:

[a gate] first and second gates formed on [an] active [region] regions of a substrate;

a field oxide formed on the substrate [adjacent the active region] between said first and second gates;

side walls formed on side surfaces of said first and second gates;

a protective layer formed on [a] said field oxide, said protective layer being a material different than said field oxide;

an insulating layer formed on the substrate including said [gate] first and second gates, said side walls, said field oxide and said protective layer;

a contact hole formed through said insulating layer; and

a connecting wire coupled to said gate through said contact hole.

7. (Amended) The semiconductor device of [clam] claim 6, wherein said protective layer is a polysilicon layer.

9. (Amended) The semiconductor device of claim 6, wherein said [gate is a] first and second gates are MOSFET [gate] gates.